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## (54) Level control of the signal produced by a transceiver coupled to a power distribution line

(57) The level of the signal output by a transceiver of digital information coupled to a power distribution line during a transmission phase is regulated by comparing the current level (Iref) of said output signal with a pre-established minimum threshold (IL) and a pre-established maximum threshold (IH); reducing the current level (Iref) when said maximum threshold (IH) is exceeded by reducing the gain; and passing to a voltage mode control of said output signal when the current level (Iref) of the output signal becomes lower than said minimum threshold (IL).

The architecture of a coupling interface implementing the above method is illustrated.

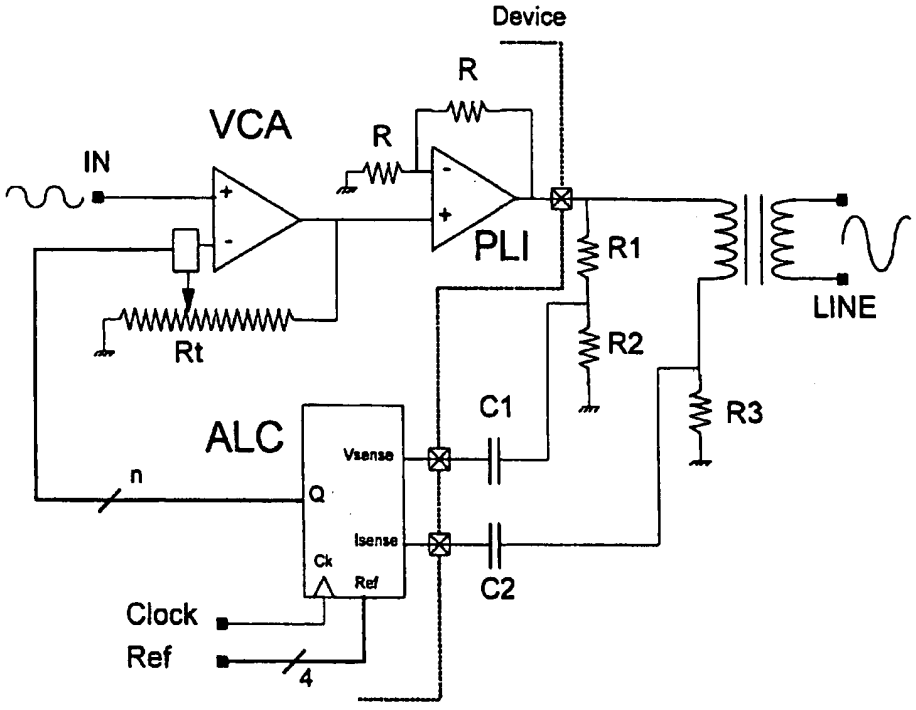


Fig. 2

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## Description

### FIELD OF THE INVENTION

**[0001]** The invention relates in general to data transmission systems and in particular to an interface circuit for coupling transceivers to power distribution lines.

### BACKGROUND OF THE INVENTION

**[0002]** Electric power distribution networks are diffused in large areas of the world. Mainly, they serve to convey and supply electric power and their possible exploitation as media for transmitting information is well known.

**[0003]** Such a medium of transmitting data is notably advantageous for communicating with users located in remote areas. Given that the majority of these users somehow have appliances and instruments connected to a power distribution line, the relevant costs of installing a dedicated line for conveying information may be avoided.

**[0004]** The feasibility of this type of data transmission, referred to as "conveyed waves", benefits from the fact that electric power is distributed with a well established frequency. The techniques of transmitting-receiving signals are based on the modulation of a carrier frequency with the signal to be sent thus allocating such a signal to a certain frequency band unoccupied by other signals. Therefore, is substantially possible to send on the same power line more signals occupying frequency bands that do not overlap with each other, having the possibility to select only the desired signal band during the reception phase.

**[0005]** The transmission of information on power distribution lines excellently suited for sending to particular site control signals for the appliances installed in those premises, without relaying on telephone lines or on radio transmissions.

**[0006]** Transmission or reception of data signals on a power distribution line requires the use of a suitable interfacing circuit between the line and the transceiver to efficiently inject a modulated carrier in the power distribution line.

**[0007]** Indeed, one of the problems in transmitting information on power lines is that the impedance of the medium of transmission is inconstant, and the variations may be of several orders of magnitude depending on the presence or absence of loads connected to the power line.

**[0008]** In order to reduce the problems due to the extreme aleatory character of the line impedance, the document DH028 issued by ENEL in September 1992, states that in Italy the control of the level of the signal output by a transceiver coupled to a power distribution line should be implemented in a current mode when the impedance is below a certain value that in the particular recommendation if fixed to 5Q, and in a voltage when the impedance is above that value.

**[0009]** The known interface circuits can either control the level in current mode or in voltage mode, as described in the US patent 4,636,771, and therefore they must be chosen in function of the prevailing line impedance condition.

**[0010]** It is evident the need or usefulness of an interface circuit that monitors the impedance of the line and switch automatically from a current mode to a voltage mode of controlling the signal to be injected on a power distribution line and viceversa, depending on the actual impedance of the line.

### OBJECT AND SUMMARY OF THE INVENTION

**[0011]** It has now been found and is the object of the present invention a new method and a relative circuit for controlling the level of the output signal produced by a transceiver of digital data coupled to a power distribution line capable of switching automatically from a current mode to a voltage mode and viceversa, depending on the sensed impedance of the distribution line.

**[0012]** The method of the invention of controlling the level of the signal produced by the transceiver of digital data coupled to a power distribution line during a transmission phase, comprises:

comparing the current level (Iref) of the signal with a pre-established minimum value (IL) and a pre-established maximum value (IH);
reducing the current level (Iref) when it exceeds the maximum value (IH) by reducing the gain;
passing to a voltage mode control when the current level (Iref) becomes lower than said minimum value (IL) and until the current level remains lower that the minimum value (IL).

**[0013]** According to a preferred embodiment, the voltage mode control is effected by comparing the voltage level (Vref) of the signal with a high (VH) and a low (VL) pre-established thresholds, and by regulating the voltage gain.

**[0014]** According to another aspect of the invention, the coupling interface of a transceiver of digital information to a power distribution line controlling the level of the signal injected on the line during a transmission phase, comprises:

a voltage amplifier (VCA) the gain of which is controlled in function of a digital datum (N) and to an input of which the signal to be transmitted is applied;
a current amplifier (PLI) coupled to the output of said voltage amplifier (VCA) delivering the signal to be injected on the line;
a first pair of comparators comparing the voltage on a current sensing resistor in series to the output of said current amplifier (PLI) with a first pair of pre-established high and low thresholds and producing

a first pair of first (A) and second (B) logic signals;
a second pair of comparators comparing a signal representing the output voltage of said current amplifier (PLI) with a second pair of pre-established high and low thresholds and producing a second pair of third (C) and fourth (D) logic signals;
a control logic circuit producing said digital datum (N) for reducing the gain of said voltage amplifier (VCA) if the first signal (A) assumes a false logic value or for maintaining the same current gain if the first signal (A) and the second signal (B) assume a true logic value or increasing, reducing or maintaining the same of the voltage gain if the second signal (B) assumes a false logic value with the fourth signal (D) or the third signal (C) assuming a false logic value or the third signal (C) and the fourth signal (D) assume a true logic value.

**[0015]** True logic value is assumed by the first signal (A) and by the third signal (C) when the relative signal does not exceed the high threshold, while a true logic value is assumed by the second signal (B) and by the fourth signal (D) when the relative signal exceeds the lower threshold.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0016]** The various aspects and advantages of the invention will become even more evident from the description of an embodiment and by referring to the attached drawings, wherein:

**Figure 1** is a diagram of line impedance-voltage level of the transmitted signal;
**Figure 2** illustrates a possible circuit diagram of the interface of the invention;
**Figure 3** is a possible circuit diagram of the gain controlled voltage amplifier of the invention;
**Figure 4** illustrates a suitable circuit for producing a digital datum N from a signal representing the level of the modulated signal to be injected on the line;
**Figure 5** is a flow chart of the algorithm implemented by the control logic circuit.

## DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

**[0017]** ENEL specifications call for a transmission characteristic according to which the output signal should be kept at a constant voltage level of 1 to 2 $V_{EFF}$ if the line impedance is greater than 5Ω, or at a current level of 200 to 400 $mA_{EFF}$ if the line impedance is lower than 5Ω.

**[0018]** This recommended transmission characteristic is depicted in figure 1 wherein the waveforms of the effective value of the voltage signal to be injected on the line depending on the line impedance arc shown.

**[0019]** In order to illustrate the functioning principle of the invention, reference is made to an embodiment of a single ended output driver, as in the example shown in figure 2. Of course, the concepts that will be described may be equally applicable to other output driver for example of a fully differential amplifying structure.

**[0020]** The interface circuit that implements the method of the invention may be realized by detecting two magnitudes Vsense and Isense, respectively representing the voltage level and the current level of the signal to be coupled to the transmission line. As depicted in the example of figure 2, this may be done by deriving a scaled replica of the output voltage signal with a voltage divider (series of R1 and R2 in the figure) connected in parallel to the output, and obtaining an Isense voltage signal proportional to the current level of the output signal by placing a current sensing resistor R3 in series to the output.

**[0021]** Naturally, the signals Vsense and Isense may also be differently produced, for example, by using other equivalent integrated components instead of resistors. Moreover, since it is only necessary that such signals represent the voltage and current respectively on a load, any signal that satisfies such a requisite in the interface may be sensed.

**[0022]** For example, instead of sensing the output current through a sensing resistor crossed by the load current, a representative value of the output current may be obtained by using current mirrors drawing current from the output buffer of the interface (PLI).

**[0023]** Such Vsense and Isense signals are compared in a control circuit with respective threshold pairs that define the permitted maximum and minimum values of the variation interval of the current level and of the voltage level of the output signal to be coupled to the power line. The control logic circuit produces, according to the method of the invention, a digital datum N that is input to a VCA (Voltage Controlled Amplifier). The VCA amplifies the signal on the IN input to be transmitted, by a quantity established by the digital datum N, feeding the signal so amplified to a second amplifier having a high current gain. At the output of the interface PLI, the signal is coupled to the power line.

**[0024]** The circuit of the VCA may be as shown in figure 3. Substantially, it is an operational amplifier with negative feedback, realized by a series of resistors constituting a voltage divider, the taps of which have switches for connecting or disconnecting them to an inverting input of the operational amplifier. The digital datum N produced by the control circuit is fed to a decoder which, correspondingly control the switches of the voltage divider, for modifying the feedback factor and thereby the voltage gain.

**[0025]** A possible embodiment of the control system is illustrated in figure 4. Vsense and Isense are alternate signals because they are proportional to the voltage level and to the current level of the signal being coupled to the power line. They are rectified and integrated in order to obtain DC signals Vref and Iref proportional to their

amplitudes. This may be effected, as shown in the figure, using a diode connected in series to a low pass R-C filter or by using any other circuit outputting a DC voltage proportional to the amplitude of the respective alternate input signal.

**[0026]** Iref and Vref are then compared with respective high and low thresholds, by the use of four comparators that produce the logic signals A, B, C, D. The LOGIC block processes the signals output by the comparators and controls an Up/Down counter whose output provides the digital datum N.

**[0027]** The counting of the Up/Down counter is timed by a clock signal having a lower frequency than the frequency of the modulating signals.

**[0028]** The algorithm of the invention is schematically summarized in figure 5. At start, the possibility of implementing a current mode control is prioritarily assessed by comparing Iref with the high and low thresholds, IH and IL respectively.

**[0029]** If Iref is greater than the low threshold IL, the current gain is kept constant or reduced depending on whether Iref is lower or higher than the IH high threshold.

**[0030]** However, if Iref is lower than IL, that is, if the current level of the signal coupled to the output is lower than a minimum value, then this means that the impedance of the distribution line is higher than the maximum value established for using a current mode control and it is necessary to switch to a voltage mode control.

**[0031]** The voltage mode control is simply effected by varying the voltage gain of the VCA so that the signal Vref remains between the VL and VH thresholds.

## Claims

1. A method of regulating the level of the signal output by a transceiver of digital information coupled to a power distribution line during a transmission phase comprising

   comparing the current level (Iref) of said output signal with a pre-established minimum threshold (IL) and a pre-established maximum threshold (IH);
   reducing the current level (Iref) when said maximum threshold (IH) is exceeded by reducing the gain;
   passing to a voltage mode control of said output signal when the current level (Iref) of the output signal becomes lower than said minimum threshold (IL).

2. The method according to claim 1, wherein said voltage mode control is carried out by comparing the voltage level (Vref) of said output signal with a pre-established low threshold (VL) and a preestablished high threshold (VH) thresholds and regulating the gain to maintain the voltage level (Vref) within said thresholds.

3. A coupling interface for a transceiver of digital information coupled to a power distribution line comprising means for regulating the level of the output signal coupled to the line during a transmission phase, characterized in that said means comprise

   a voltage amplifier (VCA) the gain of which is controlled in function of a digital datum (N) and to an input of which the signal to be transmitted is applied;
   a current amplifier (PLI) coupled to the output of said voltage amplifier (VCA) delivering the signal to be injected on the line;
   a first pair of comparators comparing the voltage on a current sensing resistor in series to the output of said current amplifier (PLI) with a first pair of pre-established high and low thresholds and producing a first pair of first (A) and second (B) logic signals;
   a second pair of comparators comparing a signal representing the output voltage of said current amplifier (PLI) with a second pair of pre-established high and low thresholds and producing a second pair of third (C) and fourth.(D) logic signals;
   a control logic circuit producing said digital datum (N) for reducing the gain of said voltage amplifier (VCA) if the first signal (A) assumes a false logic value or for maintaining the same current gain if the first signal (A) and the second signal (B) assume a true logic value or increasing, reducing or maintaining the same of the voltage gain if the second signal (B) assumes a false logic value with the fourth signal (D) or the third signal (C) assuming a false logic value or the third signal (C) and the fourth signal (D) assume a true logic value.

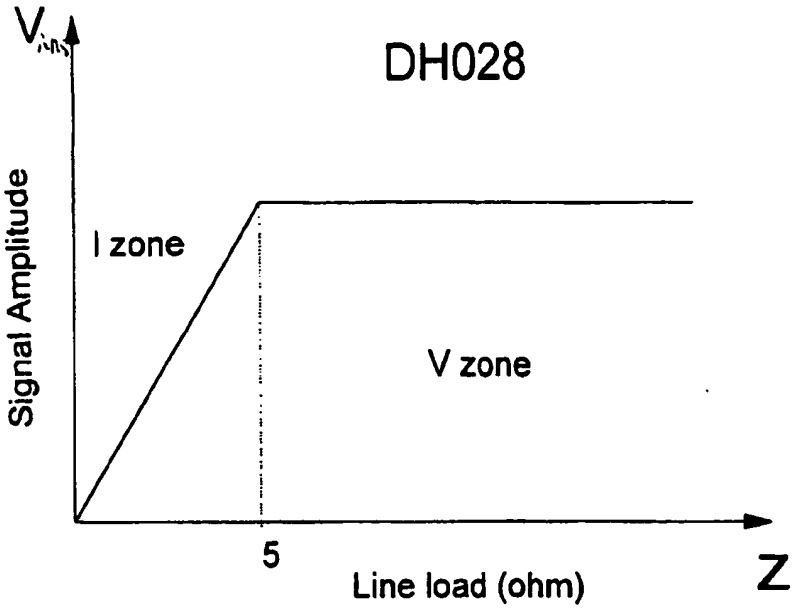
DH028
Signal Amplitude
I zone
V zone
5
Line load (ohm)
Z

Fig. 1

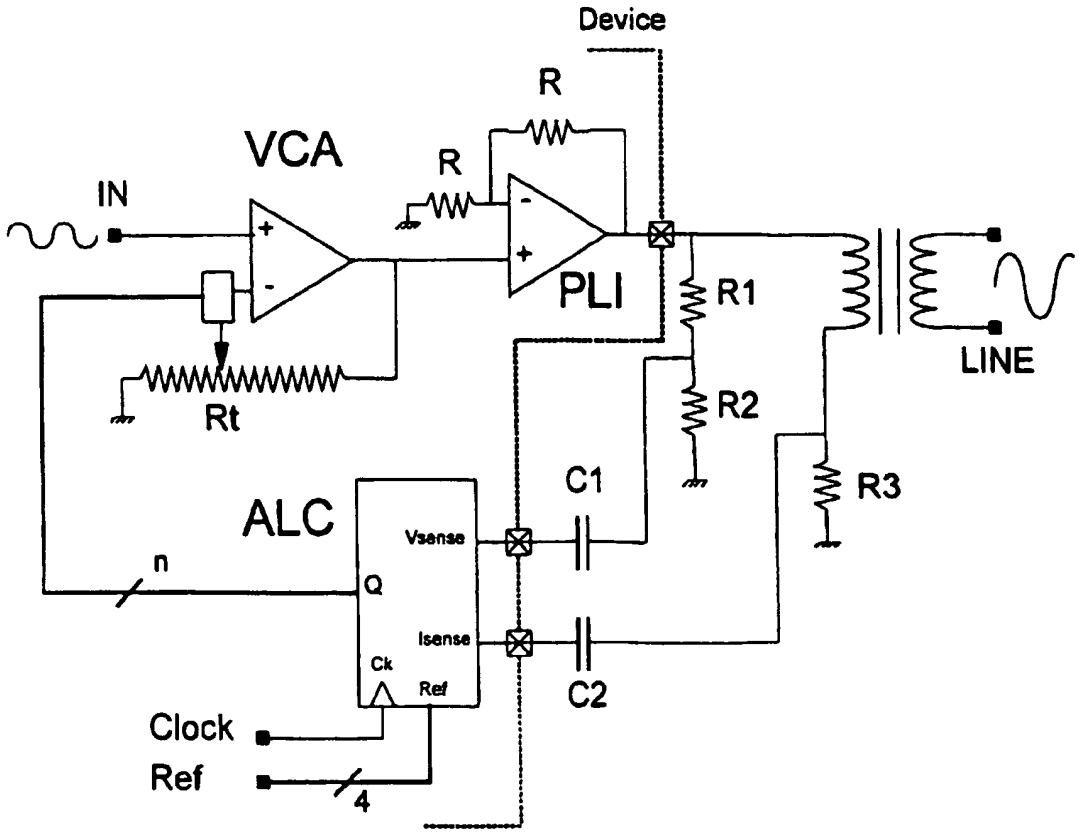
Device
R
VCA
R
IN
PLI
R1
LINE
Rt
R2
C1
R3
ALC
Vsense
n
Q
Isense
Ck
Ref
C2
Clock
Ref
4

Fig. 2

VCA

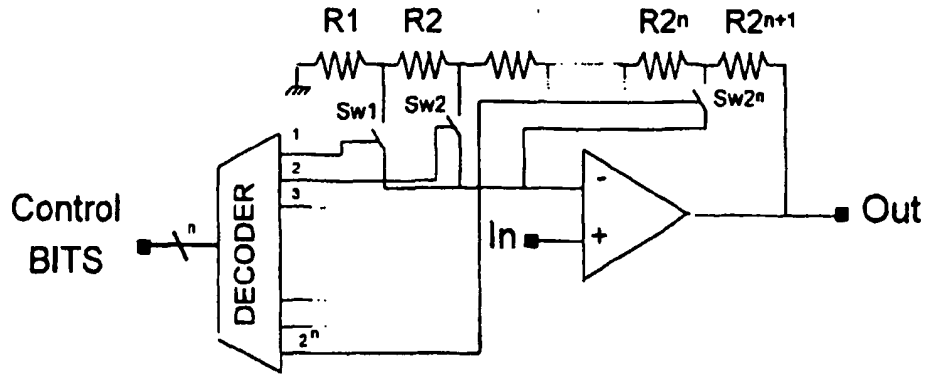


Fig. 3

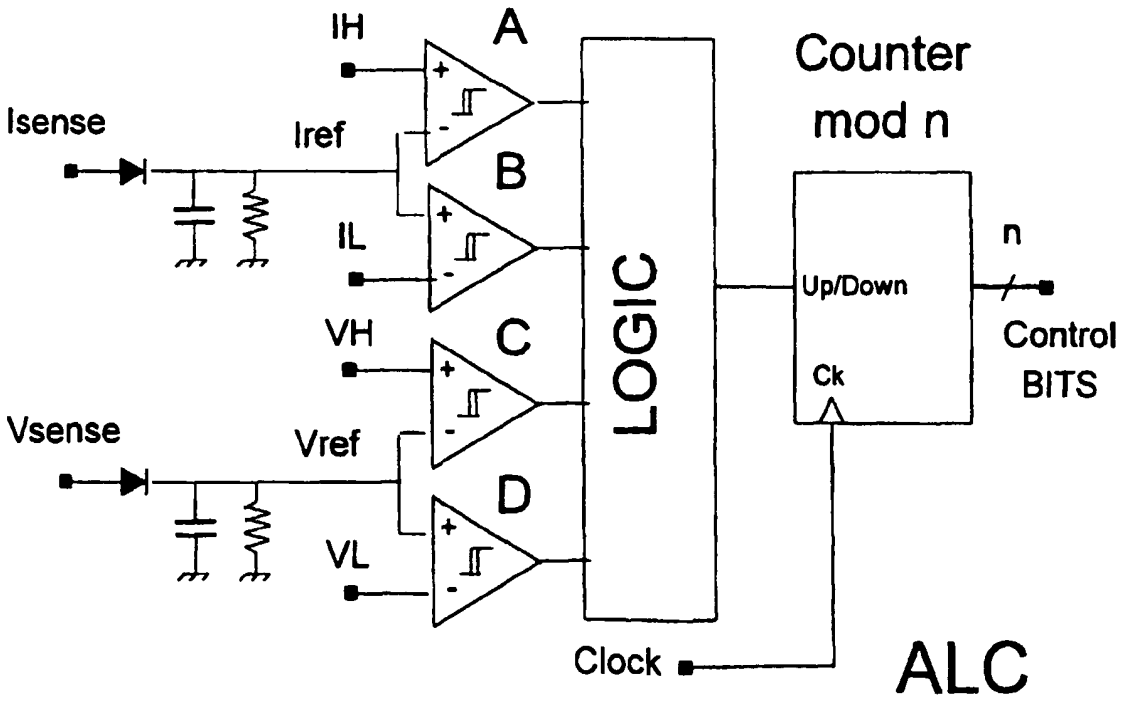


Fig. 4

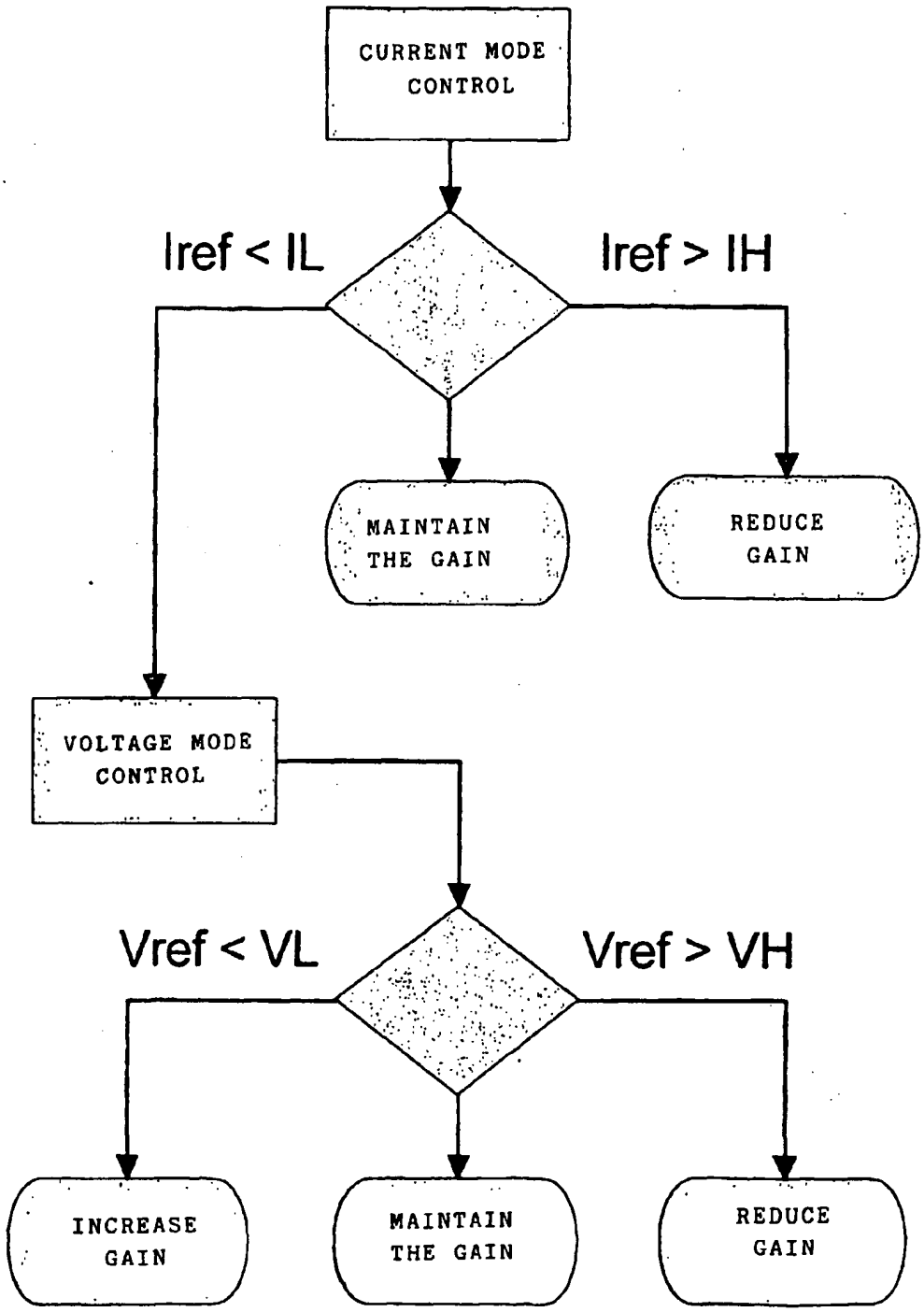
CURRENT MODE CONTROL
Iref < IL
Iref > IH
MAINTAIN THE GAIN
REDUCE GAIN
VOLTAGE MODE CONTROL
Vref < VL
Vref > VH
INCREASE GAIN
MAINTAIN THE GAIN
REDUCE GAIN

Fig. 5

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0618

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.7) |
|---|---|---|---|
| A | US 4 451 801 A (MONTICELLI DENNIS M)<br>29 May 1984 (1984-05-29)<br>* column 1, line 25 - line 28 *<br>* column 1, line 33 - line 48 * | 1-3 | H04B3/54<br>H04B3/56 |
| A | EP 0 267 887 A (ERICSSON TELEFON AB L M)<br>18 May 1988 (1988-05-18)<br>* column 1, line 22 - line 41 *<br>* column 2, line 7 - line 29; figure 1 * | 1-3 | |

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H04B

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 31 January 2000 | De Iulis, M |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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EPO FORM 1503 03.82 (P04C01)

## ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 83 0618

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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31-01-2000

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